Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **Y1**
2. **A1**
3. **B1**
4. **Y2**
5. **A2**
6. **B2**
7. **GND**
8. **A3**
9. **B3**
10. **Y3**
11. **A4**
12. **B4**
13. **Y4**
14. **VCC**

**24 mils**

**24 mils**

**2 1 14 13**

**6 7 8 9**

**3**

**4**

**5**

**12**

**11**

**10**

**HC02Y**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0035” X .0035”**

**Backside Potential:**

**Mask Ref: HC02Y**

**APPROVED BY: DK DIE SIZE .024” X .024” DATE: 2/1/16**

**MFG: FAIRCHILD THICKNESS .014” P/N: 54HC02**

**DG 10.1.2**

#### Rev B, 7/1